**4 – BIT ASYNCHRONOUS COUNTER WITH RESET OPTION:**

**Introduction to VLSI Design**

**Submitted to the**

**Dr. Masud H Chowdhury**

**Associate Professor**

**Computer Science and Electrical Engineering**

**University of Missouri – Kansas City**

By

Sahithi Gaddam

Sunayana Rapolu

Lavanya Poda

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**ABSTRACT:**

The task is fundamentally centered on the outline of essential rationale entryways utilizing rhythm and getting effective yields and the principle criteria of planning the chips in VLSI is to decrease its size as it holds the significant part in exactness particularly when parasitic capacitances are considered. To get a proficient yield, in which specific particulars are considered in picking the transistors identified with their width and length. Schematic, Symbol and Layout these three modules are outlined where format is intended to contrast the yields and without the vicinity of inward capacitances, with separate of their truth tables.

**OVERVIEW:**

Complimentary metal-oxide semiconductor (CMOS) innovation got a boundless regulation the semiconductor business which made execution upgrade and headways in circuit planning. In Cadence we first outline the schematic and image for essential rationale entryway which is confirmed for its capacity and advanced execution. At that point we outline a format of the physical circuit, checking the configuration principles to guarantee the configuration is right. The particular parameters of the transistors are considered in outlining the circuit which identify with the width and length of the chip. Two critical qualities of CMOS gadgets are high clamor insusceptibility and low static force utilization. Since one transistor of the pair is constantly off, the arrangement mix draws critical power just quickly amid exchanging in the middle of on and off states. Thus, CMOS gadgets don't deliver as much waste warmth as different types of rationale. CMOS likewise permits a high thickness of rationale capacities on a chip. It was basically thus that CMOS turned into the most utilized innovation to be actualized as a part of VLSI chips. The venture incorporate 4-bit ASYNCHRONOUS COUNTER utilizing 4 D-FLIP FLOP'S and last yields are created structure the extricated perspective of the design. The product utilized for these entryways development is Cadence Virtuoso with the NCSU outline pack. The last yields are contrasted with their individual truth tables with confirm the acquired results.

**OBJECTIVE**

To outline the schematic, image and design of 4 - BIT ASYNCHRONOUS COUNTER utilizing D – FLIP FLOP'S in Cadence apparatus and to check the usefulness of the counter through timing gap.

**INTRODUCTION:**

Counter is another class of consecutive circuits that count a progression of information heartbeats which may be consistent or unpredictable in nature (or) Counter is a semiconductor gadget that is utilized for tallying the quantity of times that an advanced occasion has happened. The counter's yield is recorded by one LSB each time the counter is timed. A paired counter is a circuit whose info is a progression of heartbeats and whose yield is parallel digits, with a different line for every force of two, 20, 21, 22, 23 et cetera, counter can be separated into double/non-twofold and synchronous/offbeat sorts. Counter can be extensively partitioned into synchronous and no concurrent sorts.

Synchronous counter has its flip-failures timed in the meantime, whilst offbeat counter is most certainly not. The clock of the former flip-failure of the no concurrent flip-lemon is sustained from the yield of the past flip-flop.

A swell counter is an offbeat counter where just the first flip-lemon is timed by an outer clock. All resulting flip-lemon are timed by the yield of the former flip-flop. No concurrent counters are additionally called swell counters on account of the way the clock heartbeat swells it path through the flip-flops. Modulus of a counter is characterized as the quantity of one of a kind expresses that a counter will arrangement through.

The MOD of the swell counter or no concurrent counter is 2n if n flip-failures are utilized. For a 4-bit counter, the scope of the tally is 0000 to 1111 (24-1). A counter may tally up or check down or number all over relying upon the information control. The check grouping generally rehashes itself. At the point when tallying up, the tally arrangement goes from 0000, 0001, 0010 ... 1110, 1111, 0000, 0001 ... and so on. At the point when checking down the include grouping goes the inverse way: 1111, 1110 ... 0010, 0001, 0000, 1111, 1110 ... and so forth.

The supplement of the include grouping tallies reverse bearing. In the event that the un-supplemented yield numbers up, the supplemented yield tallies down. In the event that the un-supplemented yield numbers down, the supplemented yield checks up.

There are numerous approaches to actualize the swell counter contingent upon the attributes of the flip failures utilized and the prerequisites of the number grouping.  Clock Trigger: Positive edged or Negative edged  JK or D flip-flops  Count Direction: Up, Down, or Up/Down Asynchronous counters are slower than synchronous counters in light of the postponement in the transmission of the beats from flip-lemon to flip-flop. With a synchronous circuit, every one of the bits in the number change synchronously with the attestation of the clock. Samples of synchronous counters are the Ring and Johnson counter. A straightforward usage of a 4-bit no concurrent counter is appeared in Figure 1, which comprises of 4 phases of fell D-flip-flops. This is a parallel counter, subsequent to the yield is in twofold framework design, i.e., just two digits are utilized to speak to the check, i.e., "1" and '0'. With just 4 bits, it can just check up to '1111', or decimal number 15.

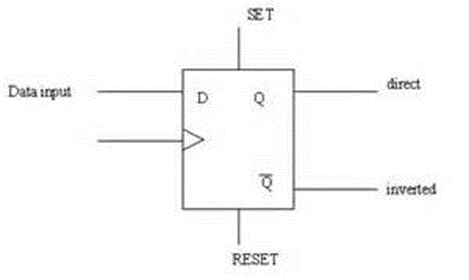
As ought to be evident from Figure 1, the inputs of all the flip-disappointments will flip between states every time they are timed. Furthermore, the yield of each flip-flop in the counter is used to clock the accompanying flip-flop. Consequently, the succeeding flip-lemon switches some place around "1" and "0" at only an expansive segment of the repeat as the flip-flop before it. Along these lines, in Figure 1's 4-bit strange counter case, the last flip-lemon will simply flip after the first flip-disappointment has starting now flipped 8 times. This sort of parallel counter is known as a 'serial', 'swell', or "no concurrent" counter. The name "unique" starts from the way this present counter's flip-disappointments are not being timed meanwhile. A 4-bit no concurrent counter, which has 16 exceptional communicates that it can number through, is moreover called a modulo-16 counter, or mod-16 counter. By definition, a modulo-k or base-k counter is one that benefits to its early on state after k cycles of the data waveform. A counter that has N flip-disappointments is a modulo 2N counter.

A no concurrent counter has a genuine downside - its pace is restricted by the aggregate spread times of the fell flip-flops. A counter that has N flip-tumbles, each of which has an engendering time t, should hence sit tight for a length of time equivalent to N x t before it can experience another move timing. A superior counter, in this manner, is one whose flip-failures are timed in the meantime. Such a counter is known as a synchronous counter.

**CIRCUIT DIAGRAM :**

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**SYMBOL:**

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**TIMING DIAGRAM:**

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Counters can depend on either the "rising-edge" or the "falling-edge" of the check heartbeat bringing about one single tally when the clock info changes state.

It may appear to be bizarre that swell counters utilize the falling-edge or rising edge of the clock cycle to change state, yet this makes it less demanding to connection counters together in light of the fact that the most critical piece (MSB) of one counter can drive the clock info of the following. This works in light of the fact that the following piece must change state when the past piece changes from high to low - the time when a convey must jump out at the following piece. Synchronous counters normally have a do and a convey in pin for connecting counters together without presenting any engendering postponements.

**DESIGN AND ANALYSIS:**

To plan a 4-bit offbeat counter in Cadence we utilize the already made D-Flip Flop and course them and utilize CMOS innovation in which we require 4 D-Flip Flops and 1 NOT door utilized for inverter rationale, which involves 1-info NOT entryway, five 2-data NAND doors.

Also, one 3-info NAND door which comprises of 14 PMOS and 14 NMOS transistors. The other 2 PMOS and 2 NMOS transistors are utilized to plan a CMOS NAND rationale mix. Along these lines yield of the CMOS NAND door is given to the inverter information which gives AND yield. For the AND entryway outline we must join PMOS transistors in the parallel association and NMOS transistors in arrangement association.

Here in this outline we think of some as particular measurements for the PMOS and NMOS transistors, for PMOS width of 4.5μm and length of 600nm and for NMOS width of 1.5μm and least length of 600nm. Where we have to consider the width of the PMOS 3 times the NMOS as the transporter engendering of openings in PMOS is little than electrons in NMOS.

For PMOS: W=4.5 u M; L=600 n M; (W/L) = 7.5

For NMOS: W=1.5 u M; L=600n M; (W/L) = 2.5

Reproductions for diverse qualities are watched and they can't pull the yield and the PMOS width is balanced likewise as the estimations appeared above and accomplished the proficient yield. We likewise realize that the float current relies on upon the span of transistor. We need to change it as per our outline.

The voltage beats for the both transistors are given taking after qualities. A deferral of 30n s is kept up between the two heartbeats to contrast and the table.

By applying legitimate ground and vdd alongside the inputs, we can dodge the shorts in the circuit so that further clamor is lessened in the circuit. In outlining the design, we ought to fare thee well in a percentage of the viewpoints like associating metal and poly with the connector M1-POLY, making n-well, checking inputs and yields and so forth. We need to check dependably with DRC to confirm the mistakes. When we finished with our design we need to concentrate it and fortify for results. These outcomes are contrasted and the AND truth table.

First, we design a symbol for inverter and NAND gate which make our schematic simple

**INVERTER:**

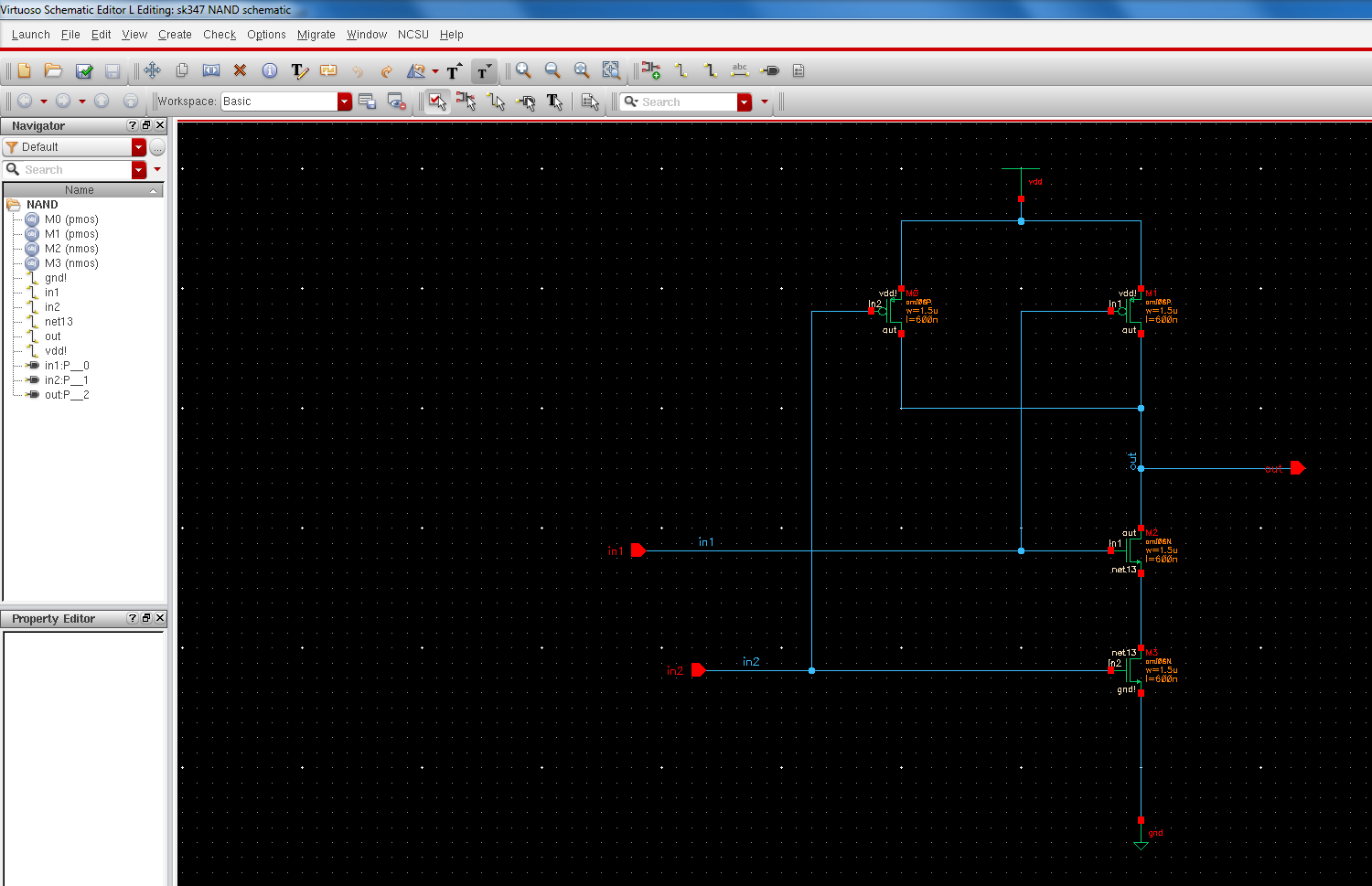
**SCHEMATIC:**

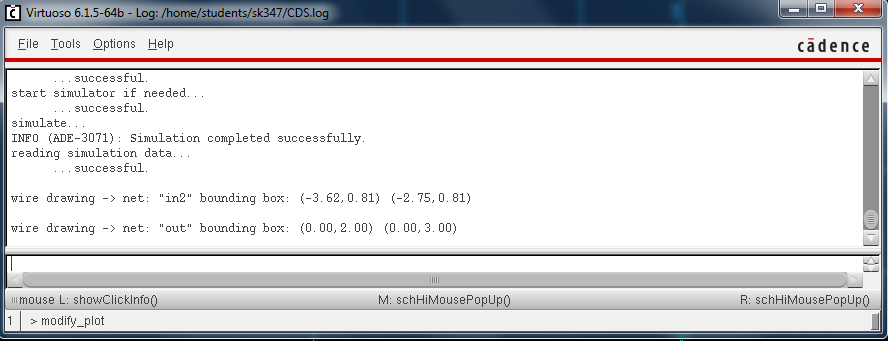
**OUTPUT:**

**SYMBOL:**

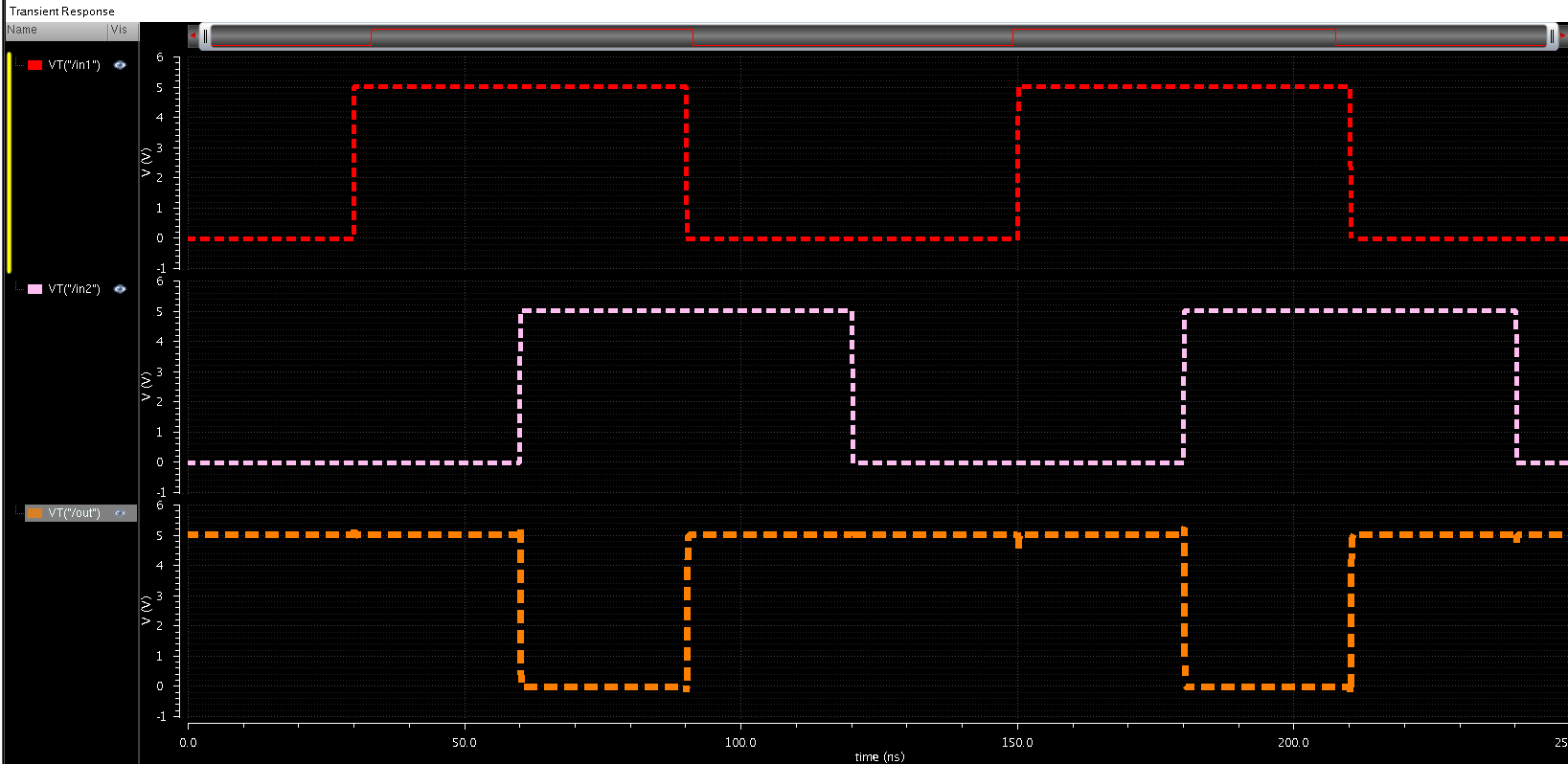
**NAND GATE:**

**SCHEMATIC:**

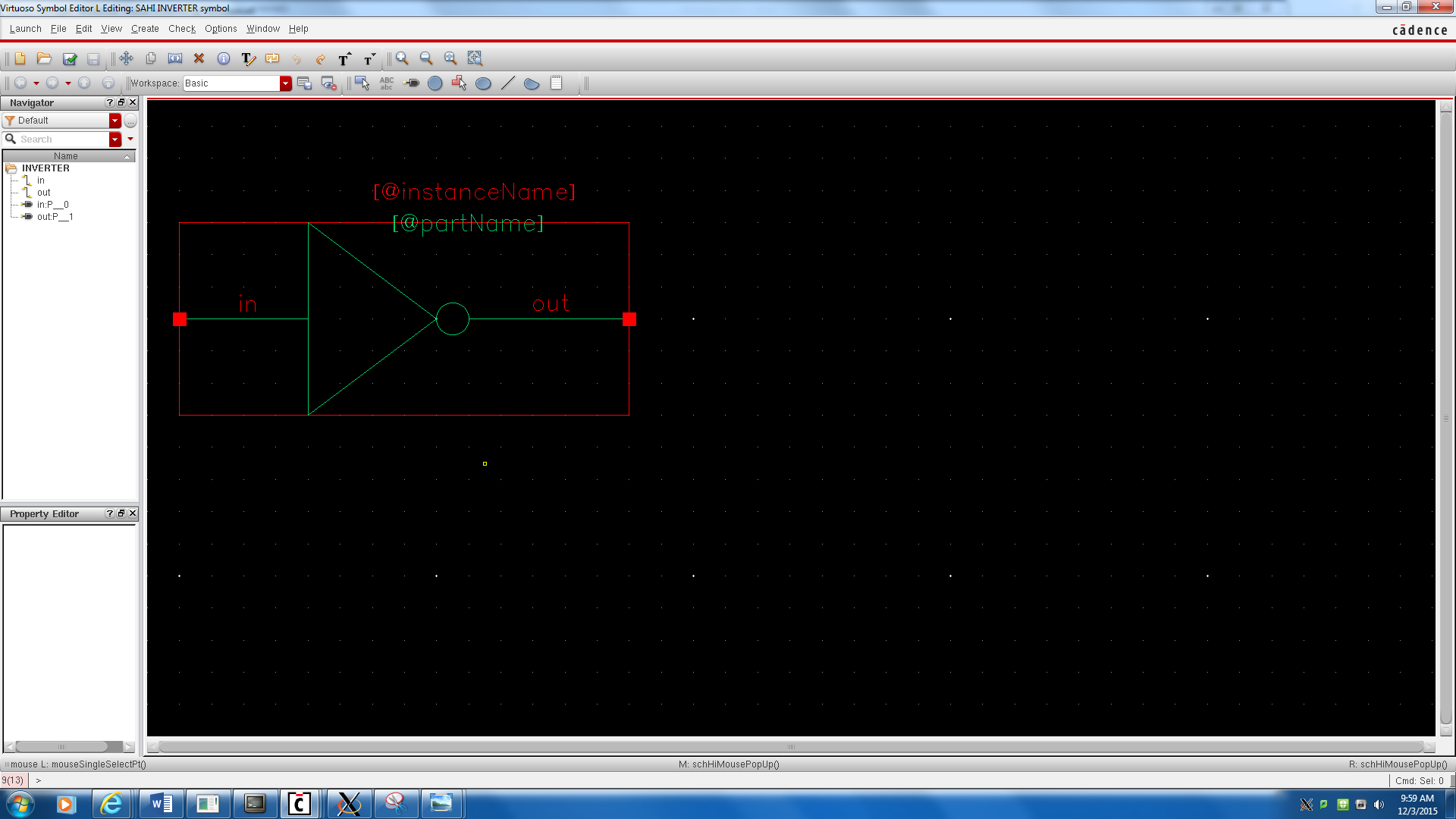




**OUTPUT:**

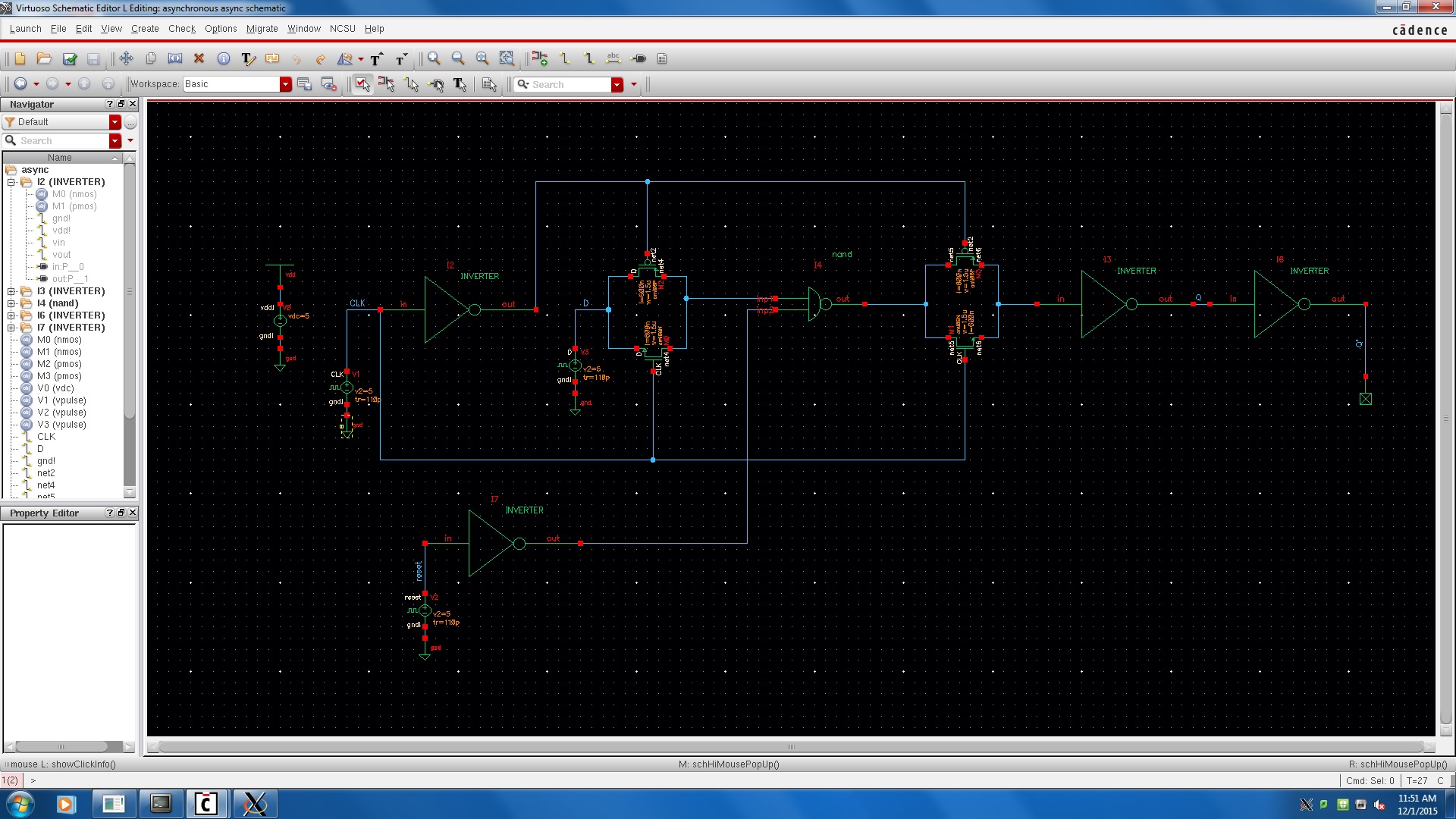


**SYMBOL:**

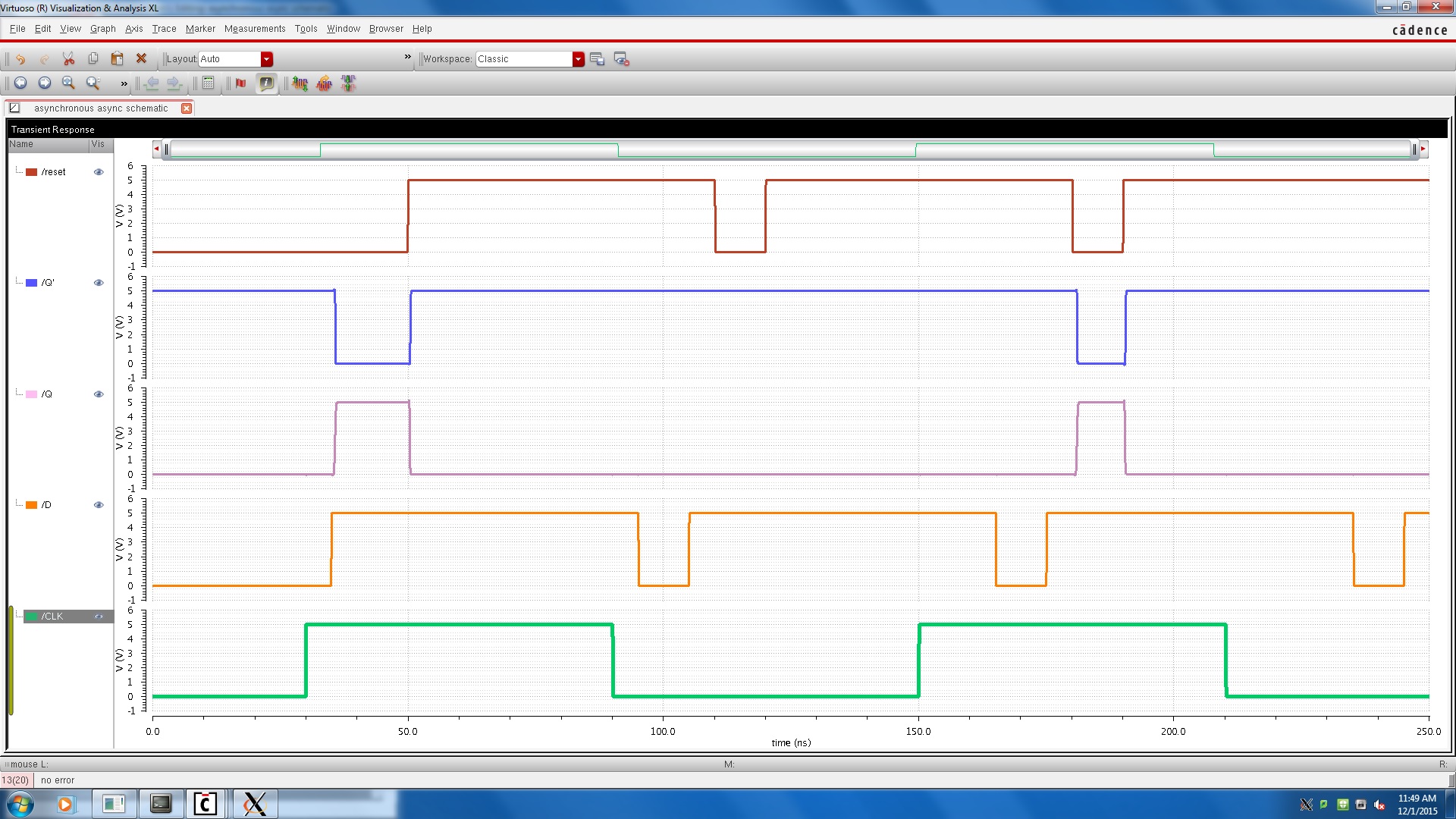
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**NAND :**

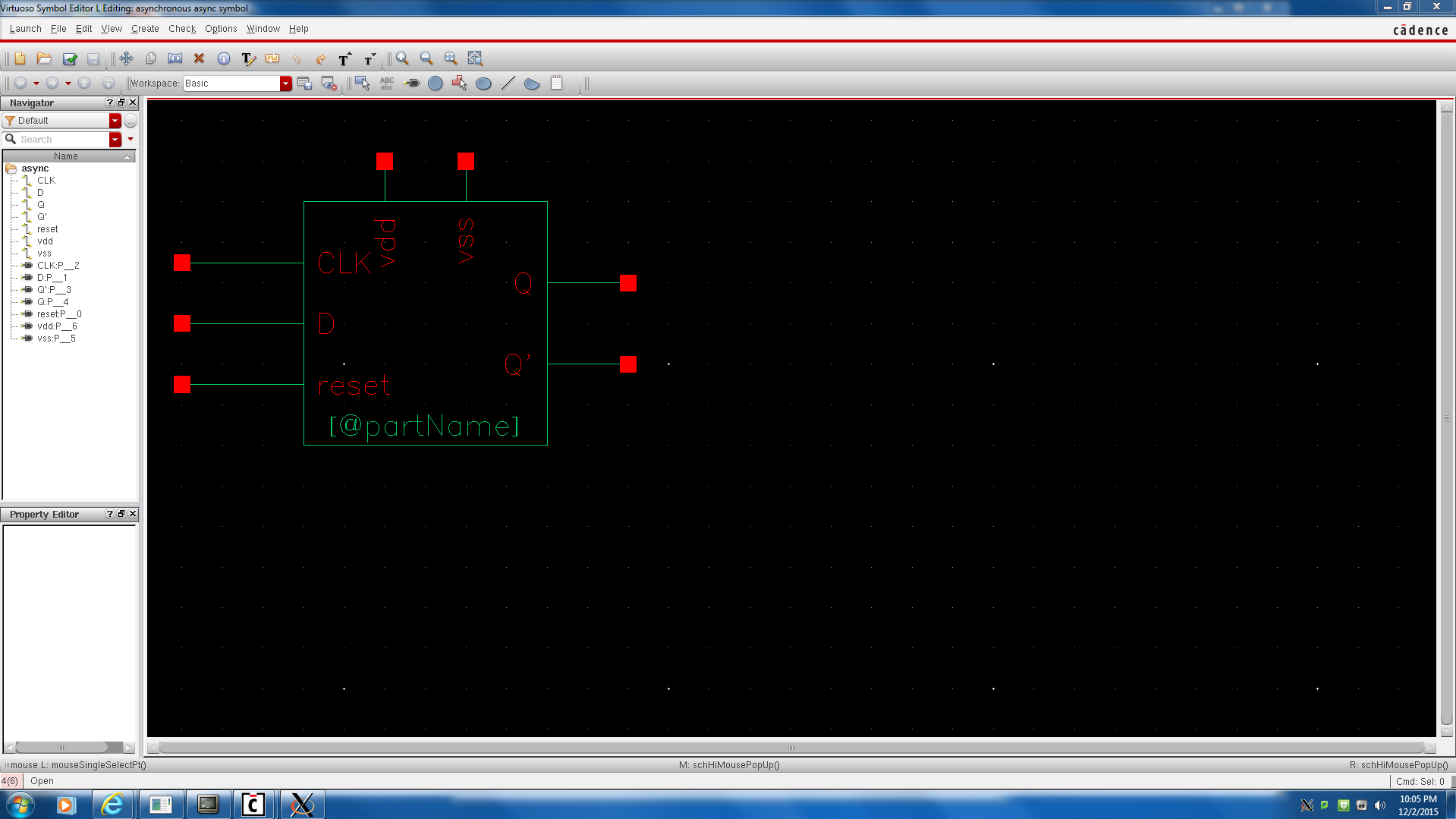
**SCHEMATIC:**

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**OUTPUT:**

****

**SYMBOL :**

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**TIMING DIAGRAM :**



In the above chart,

i. At edge An, information is low, and despite the fact that there is a positive heartbeat amid the clock period, Q (yield) stays low.

ii. At edge B, information is high and Q goes high.

iii. At edge C, information is still high and Q stays high.

iv. At edge D, information is still high and Q stays high.

v. Amid clock beat D, information goes low for a period, yet Q stays high.

vi. At edge E, information has gone low and Q goes low.

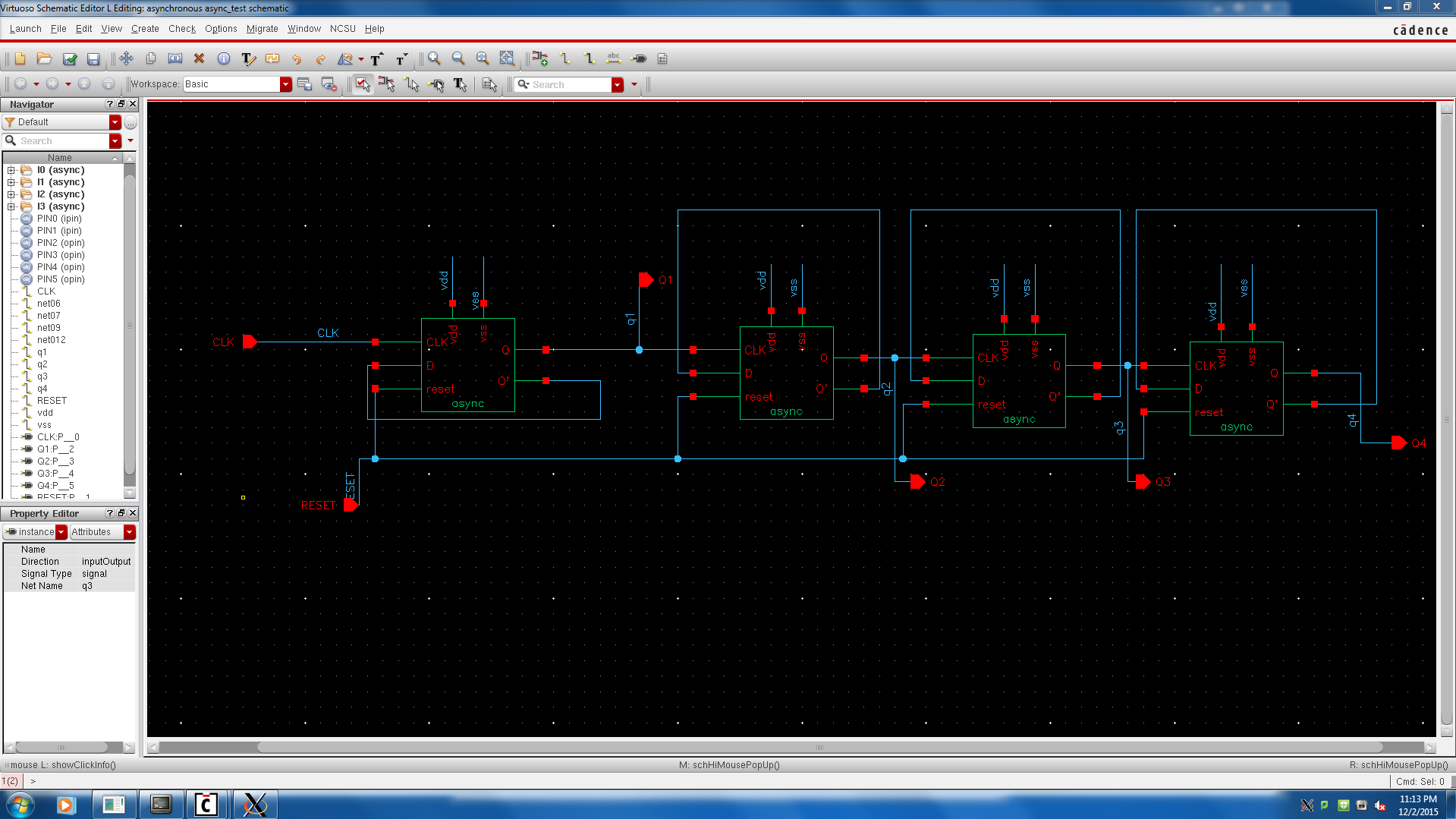
vii. Information goes high for a period amid clock beat E, yet Q stays low.

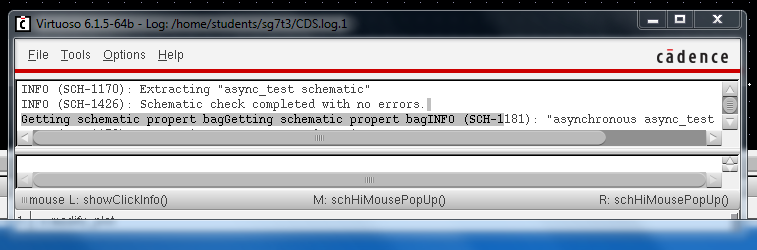
viii. At edge F, information is still low and Q stays low.

To outline D-Flip Flop I have utilized five 2-info NAND doors and a 3-information NAND entryway. I am instantiating the NAND doors which I have done in the past undertaking. The schematics of NAND entryways are appeared previously.

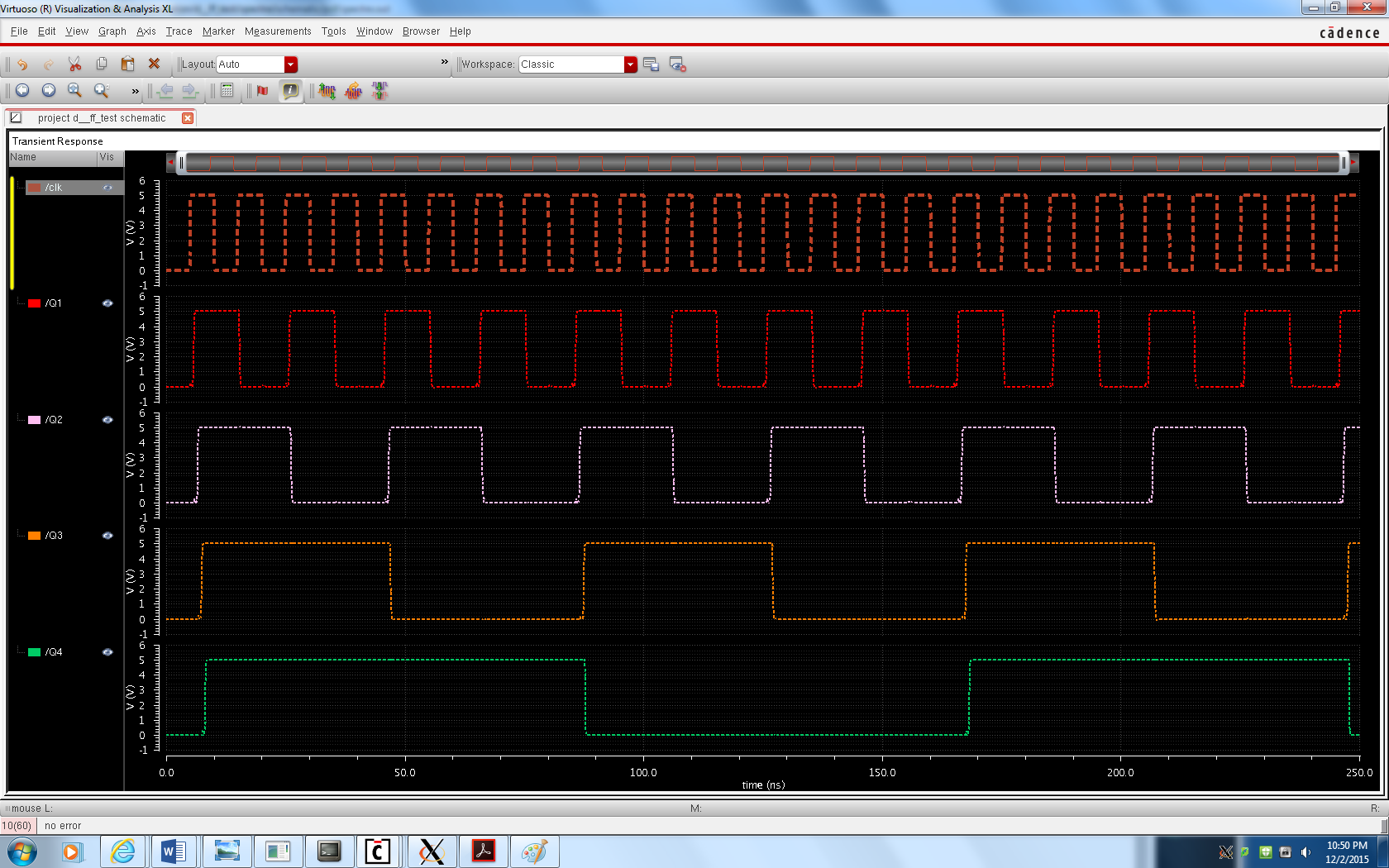
**4 – BIT ASYNCHRONOUS COUNTER:**

**SCHEMATIC:**

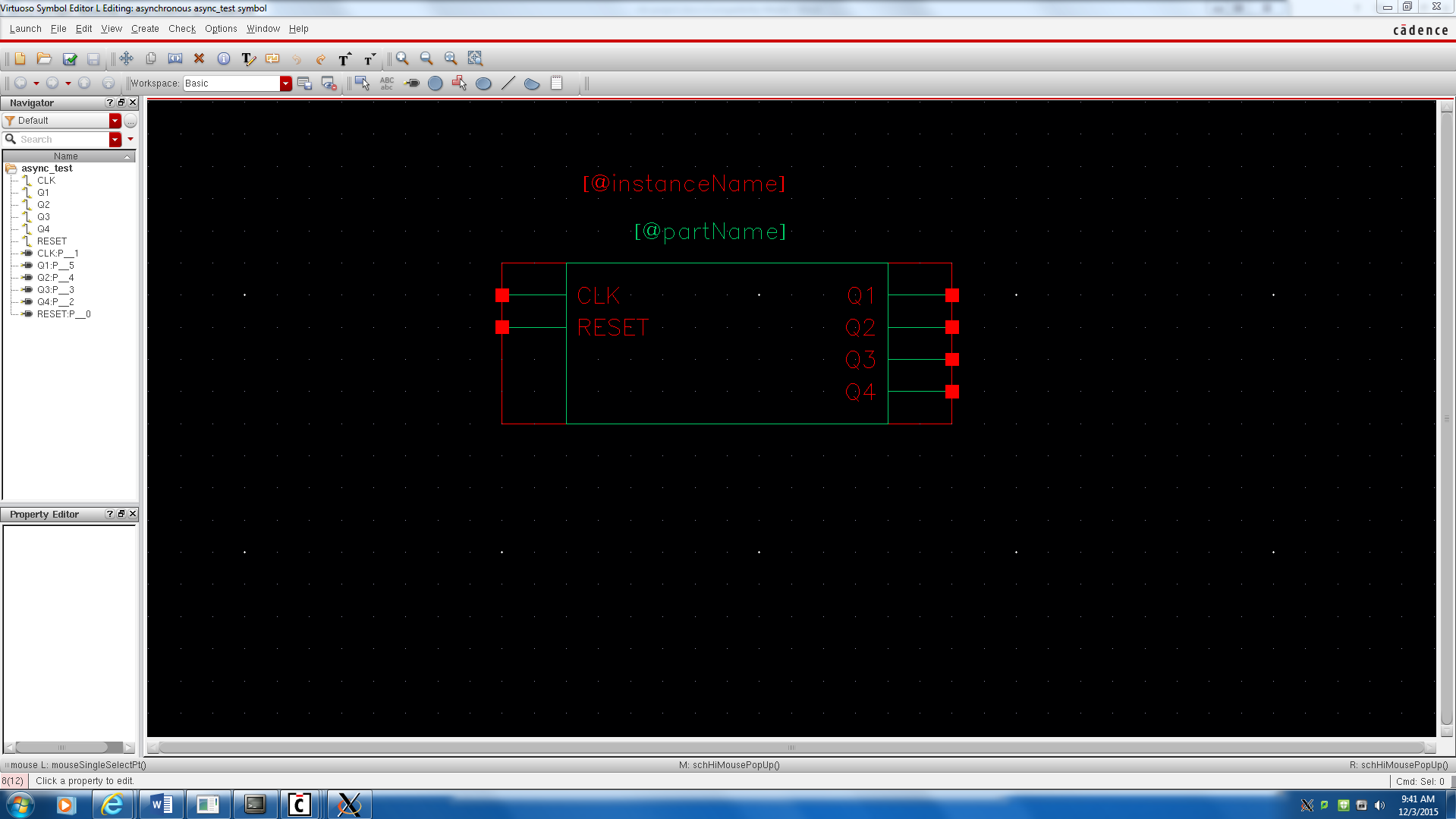
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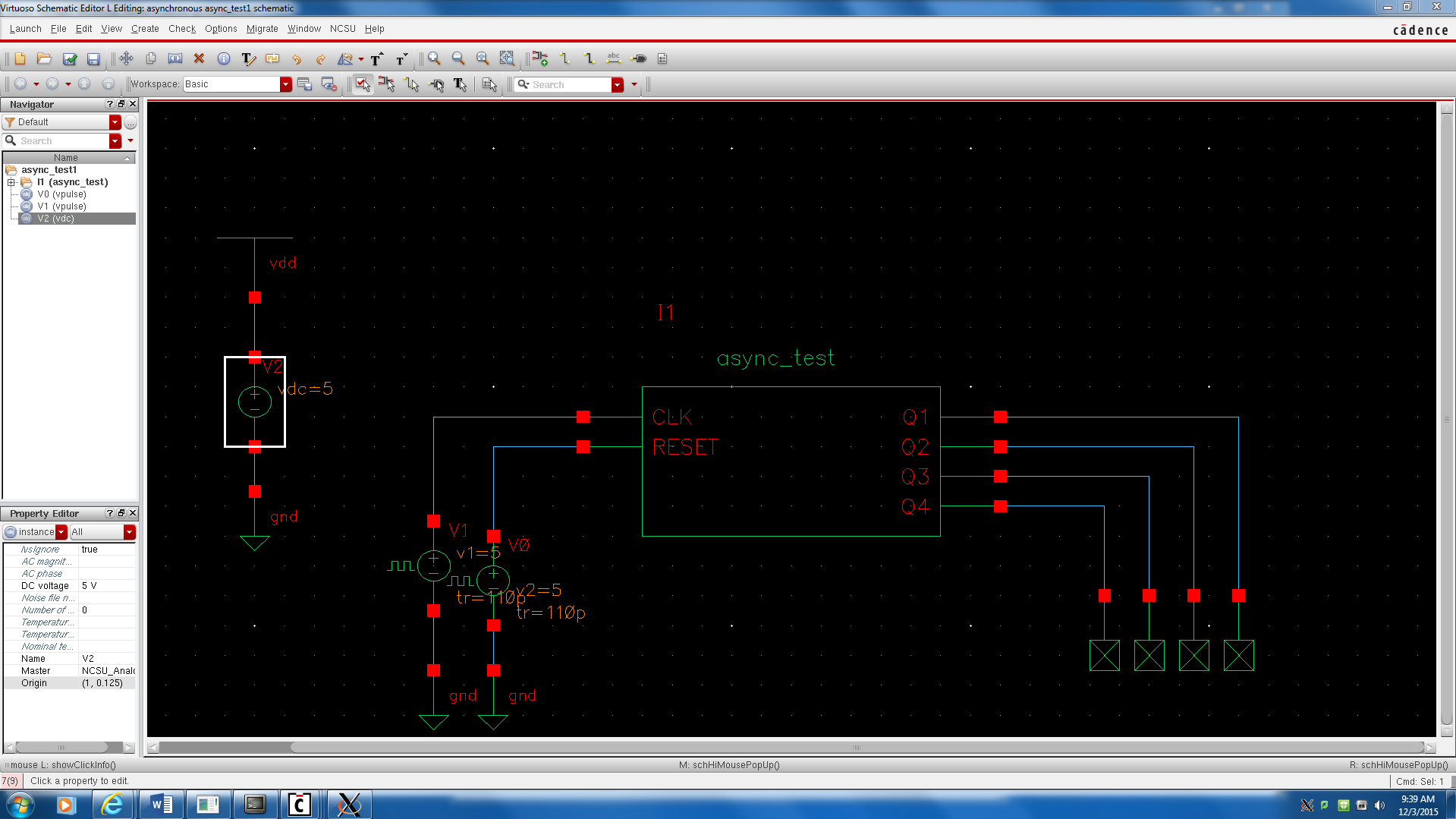
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**OUTPUT:**

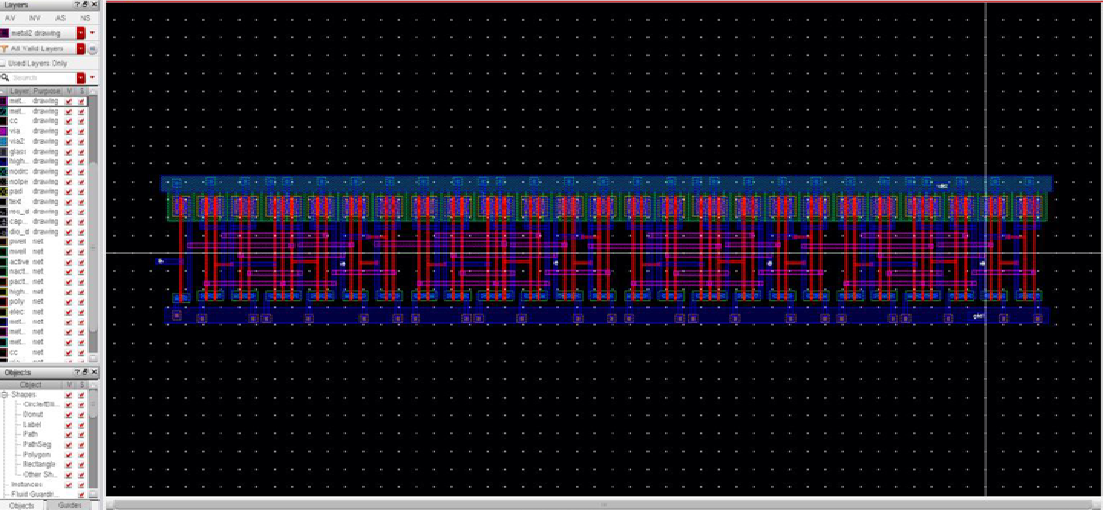
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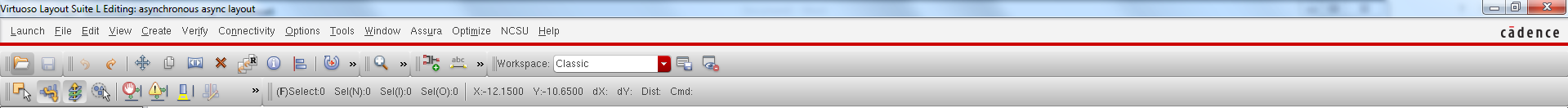
**SYMBOL:**

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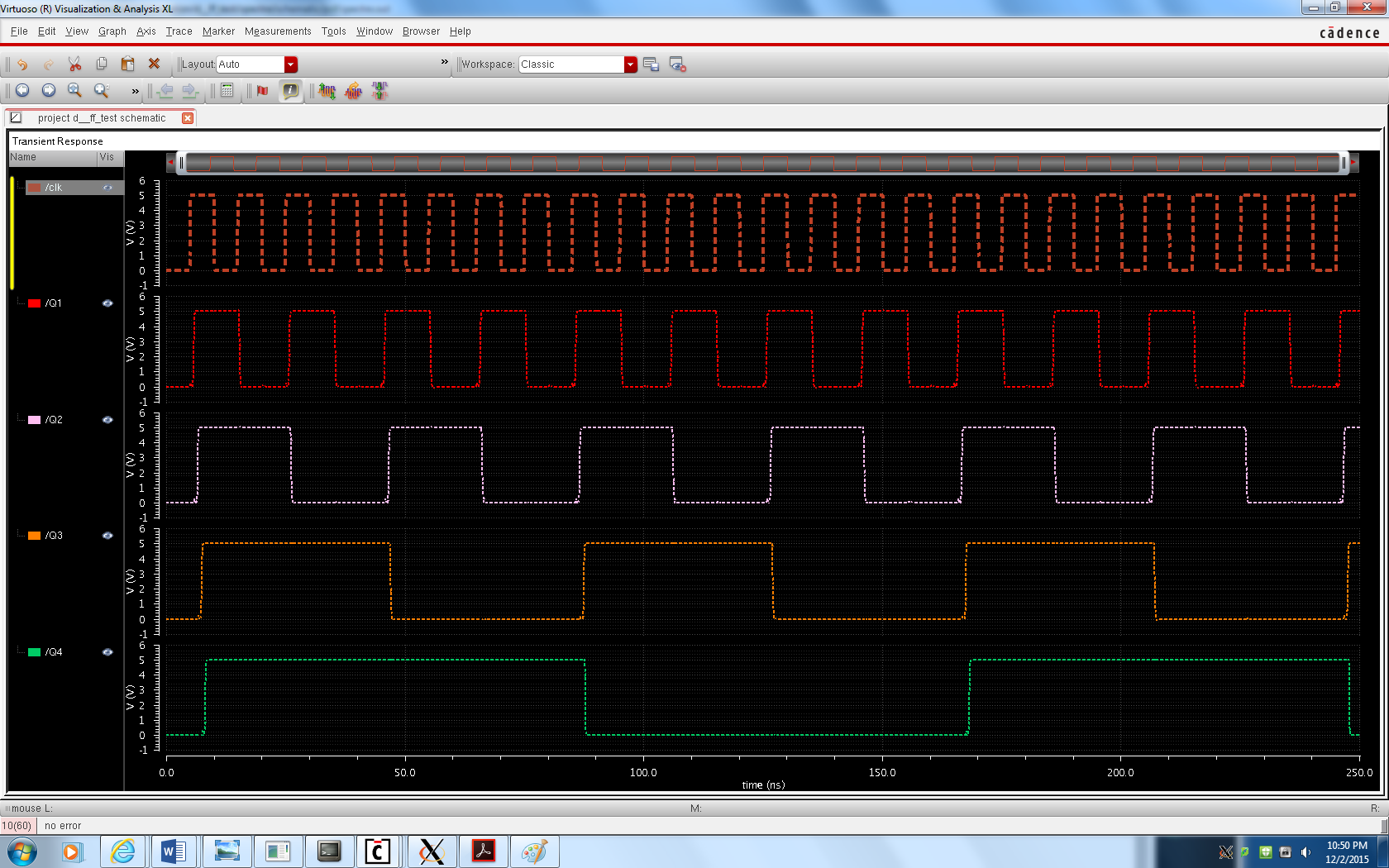
**SCHEMATIC :**

**LAYOUT:**

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**OUTPUT:**

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**Analysis and Calculations**

Rise Time and Fall Time Calculation:

Rise Time: The time between 10% and 90% points of waveforms.

Fall Time: The time between 90% and 10% points of waveforms.

|  |  |  |
| --- | --- | --- |
|  | Rise time | Fall time |
| Q1 | 0.263ns | 0.34ns |
| Q2 | 0.98ns | 0.28ns |
| Q3 | 0.99ns | 0.586ns |
| Q4 | 0.85ns | 0.92ns |

Table 1.6 Rise Time and Fall Time

Calculation of Average Power Dissipation:

The Average power Dissipation is calculated by using calculator. The step to step procedure is as follows:

Select any output signal and Open Calculator. In functional panel select special functions.

Select pavg set range and then click OK

Click Evaluate Buffer and then display in table

The average power dissipation values for Q1=2.12, Q2=2.52, Q3=3.152,

Q4=3.54 watts respectively

**Size of the Circuit Calculation:**

Width of the Layout= 250.95µm

Height of the layout= 41.25µm

Area= width\*Height= 250.95\*41.25

=10351.6875µm2

**Delay of the Circuit Calculation:**

|  |  |  |  |
| --- | --- | --- | --- |
|  | tPHL | tPLH | tp |
| Q1 | 0.147ns | 0.53ns | 0.3235ns |
| Q2 | 0.22ns | 0.46ns | 0.81ns |
| Q3 | 0.125ns | 0.60ns | 0.4625ns |
| Q4 | 0.15ns | 0.81ns | 0.46ns |

**AREA ANALYSIS :**

In the range investigation we figure the region by computing its result of length and width as appeared in screen shot beneath for 4-bit Asynchronous counter. To be best circuit we must lessen the zone however much as could be expected. The range is likewise significant criteria in outlining the circuit and the wiring use should likewise be less and short.

In my configuration of 4-bit Asynchronous counter I got length = 250.95 μ.

What's more, width = 41.25 μm

The zone = length\*width

= 250.95\*41.25 Area = 10351.6875 nm

**SPIKE REDUCTION :**

In this 4-bit Asynchronous counter there are 112 transistors, which decrease the velocity of the circuit by the inside capacitors. Along these lines, we can utilize capacitors at the yields which sets aside some an opportunity to charge and release.

We can decrease the spikes in another path by expanding the ascent and fall times.In this undertaking we can utilize capacitor of 20f Farad at the yield of 4-bit Asynchronous counter to decrease the spikes if any at the yield waveforms.

**POWER ANALYSIS :**

Dispatch ADE\_L and make another test and for DC examination select investigation as DC and Under Sweep variable check Component Parameter then tap on \Select Component". Go to the schematic window on the off chance that it is not before you, now select the voltage source associate with the Drain (V1) by tapping on it and pick DC voltage parameter. For scope range we will swing the channel voltage from 0 to 5.

For current count of individual doors add another yield to be plotted on schematic and select the negative red terminal of the Drain voltage of every entryway where yield is associated. We need to ascertain the force for every entryway and for aggregate force we must include all the individual forces of all doors.

In this venture 4-bit Asynchronous counter I have utilized 4 D-Flip Flop's and an inverter by falling them to frame a 4-bit Asynchronous counter where here I have to ascertain the current for the every flip tumble then increase with 4 since I have utilized 4 D-flip flop's furthermore for inverter then include the aggregate present and after that duplicate into 5 i.e., the vdc voltage, to get the force utilization of the 4-bit Asynchronous counter.

The current of the every D-Flip Flop is

= (20p+3.5p+7.5p+9p+20p+8p)

= 68p A.

The current for the four D-Flip Flop's is

= 68p A\*4

= 272p A.

The current of the inverter is

= 2.5p A.

The total current of the 4-bit asynchronous counter is

= (272p + 2.5p) A.

= 274.5p A.

The total power to be calculated is total current at the output of the each gate

Total power = current \* voltage

= 274.5p A\*5

=1.3 m watts.

**TRANSISTOR SIZING :**

In this counter I have utilized four D flip-flops and in every D flip-lemon and one inverter. I am instantiating the D flip-flop which I have done in the past task. For computing the transistor sizes, we need to consider the longest way in the circuit.

Initially we have do the investigation of every D-Flip Flop and one NOT door. The above circuit is a D-Flip Flop which comprises of 6 distinctive entryway delays. The entryway G1, G2, G4, G5 and G6 will have same postponements. The entryways G3 will have diverse postponements.

At that point we have to compute the postponement for the NOT door and we need to ascertain the deferrals in separately.

Tplh (low to high move) =0.69Rpeq.CL (Load capacitance).

Then aggregate postponement is figured by utilizing: Td= (Tplh + Tphl)/2.

Tphl (high to low move) =0.69Rneq.CL (load Capacitance).

Aggregate deferral = aggregate postponement of 4 D-flip lemon + deferral of NOT entryway

= 4\*(delay of G1+delay of G2 +delay of G3 + postponement of G4 + deferral of G5+ deferral of G6) Flip Flops+ postponement of NOT entryway.

The postponement of second third fourth D-flip failures will shift as it is originating from the yield of first flip lemon in this counter we are utilizing 4 D flip-flops which is 4 times of every D flip-flop. The 4-bit nonconcurrent counter contains 4 D flip-lemon and one inverter. The aggregate deferral of counter relies on upon four D flip-lemon and one inverter.

In every D flip lemon there are five 2-information NAND entryways and one 3-data NAND door. We need to ascertain the deferral of every flip lemon. The 4-bit offbeat counter contains twenty 2-info NAND entryways, four 3-data NAND doors and one NOT entryway.

In this The Delay relies on upon fan-in square, in this D hook all entryways are having fan-in equivalent 2 so sensible postponement and it relies on upon fan-out.

We utilize the most pessimistic scenario condition in this D-flipflop

To start with we need to compute the ON resistances in this circuit.

Rn=Rno/(W/L)n and

Rp=Rpo/(W/L)p,

where Rno=Resistance of a NMOS transistor with size (W/L)n=1 and Rpo= Resistance of a pmos transistor with size (W/L)p=1.Generally the estimation of Rneq will be equivalent to Rno and the estimation of Rpeq will be equivalent to Rpo/2.

For the whole system it must be equivalent to 1

In the event that the Transistors are in parallel blend then (W/L) eq =(W/L)1 +(W/L)2+… …

In the event that the transistors are in arrangement blend the (L/W)eq =(L/W)1 +(L/W)2+… … ..

We realize that Rneq=Rno/(W/L)n and Rpeq= Rpo/(W/L)eqp

For the perfect circuits (proportion less) the estimation of the resistances of the draw up and draw down systems must be same. Am considering the perfect case for ascertaining the Rneq and RpeqSo likening both Rneq and Rpeq and substituting the supposition Rpo = 3Rno.

In this I am considering the Rp=3Rn.

The width PMOS here is 4.5μm and for NMOS it will be 1.5 μm. I have done venture on this premis.

In the 4-bit offbeat counter I have utilized 4 D-Flip Flops and an inverter in which transistors pmos ought to have higher size in light of the fact that they need to direct the current of both burden capacitor and parasitic capacitance. To direct more present transistor ought to have more size contrasted with the nmos transistor that is connected to load capacitor.

Dynamic estimating orbited nmos transistors ought to have transistor measure more than the nmos transistor. This will decrease the postponement contrasted with the uniform measuring system

Here for nmos transistor have width 1.5um, nmos transistor have width 4.5 um

Uniform estimating the nmos transistors ought to have transistor size same as that of the nmos transistor.

**WORST CASE ANALYSIS :**

In worst case analysis we have to consider the longest path in which there will be more number of gates. The most active element must be placed near to the output. As, if we place it near the output it ignores the remaining the transistors capacitors charging and discharging.Here the sizes of the transistors are calculated based on the Rp0 and Rn0 relations. In this 4 bit Asynchronous counter some gates are having fan-out equal to 4. The flip-flop inverted outputs are connected to input D pin of same flip-flop and given to the clock pin of next flip-flop. So here fan-out of output of flip-flop is 4.

Total delay depends on the total twenty 2-input NAND gates, four 3-input NAND gates and one NOT gates.

**DELAY :**

Relies on upon info designs

Low to high move

- If racket and clk both are on then postpone is tplh = 0.69\*(Rp/2)\*CL

- If one of the racket or clk is on then postpone is tplh = 0.69\*(Rp)\*CL

High to low move

- If racket and clk both are on then postpone is tplh = 0.69\*(2Rn)\*CL

Depends on fanin

Delay α 𝑓𝑎𝑛𝑖𝑛2

- In this d flip slump all doors are having fanin break even with 2 so sensible postponement

Depends on fanout

Delay α 𝑓𝑎𝑛𝑜𝑢𝑡

- In this d flip tumble all entryways are having fanout equal to 2 reasonable delay.

**RESULT :**

The yield waveforms of the 4-bit Asynchronous counter utilizing D-flip failures are checked with its particular timing outline that tallies from 0(0000) to 15(1111).

**CONCLUSION :**

The yields of the counter relies on upon the clock at whatever point the clock goes to logic1 or comes down to rationale 0. Here counter depends on the positive edge of the clock. A nonconcurrent counter is a swell counter where just the first flip-failure is timed by an outer clock. All resulting flip-failures are timed by the yield of the first flip-flop. Nonconcurrent counters are likewise called swell counters on account of the way the clock heartbeat swells it route through the flip-flops. This counter will augment once for each clock cycle and takes two clock cycles to flood, so every cycle it will substitute between a move from 0 to 1 and a move from 1 to 0. Notice this makes another clock with a half obligation cycle at precisely a large portion of the recurrence of the information clock. Along these lines, nonconcurrent counter is likewise called as recurrence divider. The recurrence is precisely isolated by 2 (f/2) with past information.

In the chip plan strategies size involved by the circuit is the significant concern. There are such a variety of imperatives in planning are Zone,Power,Delays,Inputs and yields.

From task, we can reason that the outcomes from separated perspective gives a more precise result than the schematic reproduction. Bends in the yield are overseen by contrasting the sizes of the transistors.

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http://www.electronics-tutorials.ws/counter/co